Introducing the SLVS-EC3 RX IP

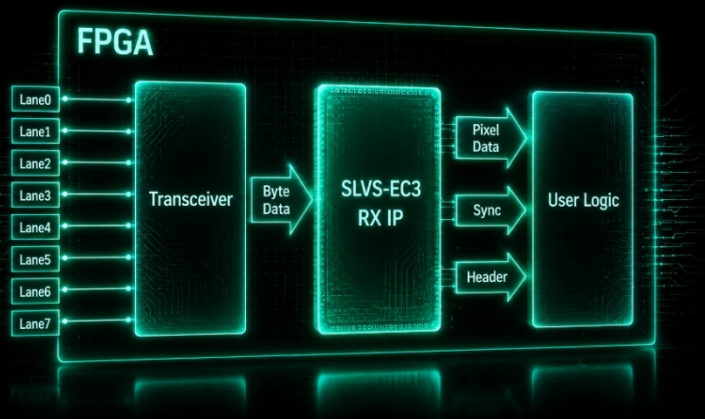
for AMD FPGAs

What is SLVS-EC?

SLVS-EC (Scalable Low Voltage Signaling with Embedded Clock) is a high-speed interface developed by Sony for image sensors. Since the clock is embedded in the data, no dedicated clock lines are required, simplifying PCB design for high-speed serial interfaces. Starting with Version 3.0, GCC (Gigabit Channel Coding), a highly efficient coding scheme, was introduced to enable data transmission with lower overhead than conventional 8B10B coding. Version 3.1 further increases the maximum data rate to **12.5 Gbps per lane**.

SLVS-EC3 RX IP Overview

Developed by CIS, the SLVS-EC3 RX is a simple IP core that extracts pixel data from byte data received through an FPGA high-speed transceiver. It supports SLVS-EC Version 3.1, including payload error detection and optional payload error correction, while being designed with an emphasis on low resource utilization. By combining the IP with your own logic, overall system resource utilization can be optimized.



Key Specifications

Item	Specification
SLVS-EC Version	3.1 Compliant
Lane	1, 2, 4, 6, 8
RAW Bit Depth	8, 10, 12, 14, 16
Line Length	4 – 65532 (multiples of 4)
Input Data Width	32, 64
Coding	8B10B, GCC
CRC	Supported
ECC	Supported (optional)
Baud Rate	Up to 12.5 Gbps/lane
Multi Stream	Not Supported
Output Signals	Pixel Data, Sync. Signals, Packet Header etc.
Devices	AMD 7-Series, AMD UltraScale, AMD UltraScale+

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Resource Utilization

One of the key features of the SLVS-EC3 RX is its low resource utilization. Resource usage varies depending on factors such as the input data bus width, maximum number of lanes, and whether error correction is enabled. The tables below show the resource utilization for each configuration using a Kintex UltraScale+ device with Vivado 2025.2. Although the IP supports dynamic lane-count configuration, resource usage can be further reduced by fixing the number of lanes used.

Input Data Bus Width = 32 bit/lane (ECC enabled in parentheses)

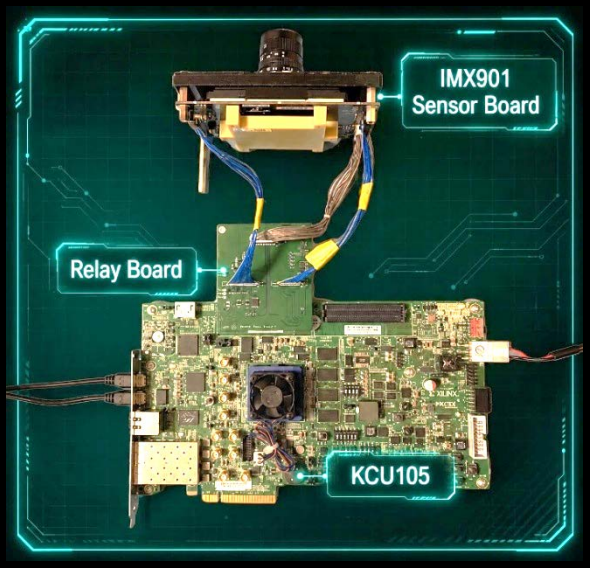
Resource	1 Lane	2 Lane	4 Lane	6 Lane	8 Lane
LUT	3077(4919)	4919(6692)	8743(10914)	14429(19871)	18081(23592)
FF	1602(3654)	2418(4377)	4333(7044)	6781(11137)	8394(12767)
BRAM	0(4.5)	0(4.5)	0(7.5)	0(13.5)	0(13.5)

Input Data Bus Width = 64 bit/lane (ECC enabled in parentheses)

Resource	1 Lane	2 Lane	4 Lane	6 Lane	8 Lane
LUT	4718(7323)	8083(10755)	16983(22081)	28884(40520)	35866(47509)
FF	2848(5558)	4644(7353)	8908(13270)	14233(22355)	17864(25994)
BRAM	0(7.5)	0(7.5)	0(13.5)	0(34)	0(34)

Demonstration Environment

CIS provides a relay board for connecting a Sony IMX901 sensor board to an AMD KCU105 evaluation board, as shown in the photo on the right, along with a reference design that runs on the KCU105. This setup supports demonstrations of RAW10 and RAW12 formats with up to four lanes. The reference design can be freely customized to meet your application requirements. CIS can also propose solutions for other configurations based on your specific requirements.



Technical Support

CIS has a team of experienced engineers with expertise in RTL design for various high-speed interfaces and image processing, PCB design involving high-speed signals, and embedded software development. Please feel free to contact us regarding IP evaluation environments, customization, or other technical requirements.

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